

Technologies Enabling Custom Radiation-Hardened Component Development, Phase I

Completed Technology Project (2011 - 2011)



Project Introduction

Two primary paths are available for the creation of a Rad-Hard ASIC. The first approach is to use a radiation hardened process such as existing Rad-Hard foundries. These foundries use special processing steps to decrease the total ionizing dose issues, but do not reduce the single event effects. The second approach is to use a special standard cell library containing hardening techniques that can be built on a standard state-of-the-art commercial foundry. This cell library must compensate for the unhardened foundry by using special layout techniques to retain the ability to operate through the total ionizing dose experienced in the radiation environments. These techniques are generally referred to as radiation hardened-by-design layout techniques (RHBD). For hardening of the circuit architectures against upsets from the single event effects, both the commercial and the Rad-Hard foundries must incorporate some type of mitigation scheme requiring special transistor interconnects or redundant nodes. This program will fill this void, providing the space community with the ability to easily acquire the RHBD Micro-RDC standard cell libraries for use with commercial ASIC design flows. The library will include a full suite of IO pads designed by Micro-RDC and successfully implemented in test chip designs at 90nm and 65nm. Finally, a portion of the custom via programmable structured ASIC fabric designed by Micro-RDC and Viasic will be made available to the library users. This fabric can be embedded into a design which can be modified and reprogrammed by generating just via 3 mask layer, which can lead to a substantial cost savings over a complete new ASIC design. This program will allow Micro-RDC to transform its custom libraries into synthesis libraries, and enable other companies the opportunity to use a proven and fully characterized RHBD ASIC cell library and suite of Mega Cell hard IP for rapidly developing spaceborne systems.



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Table of Contents

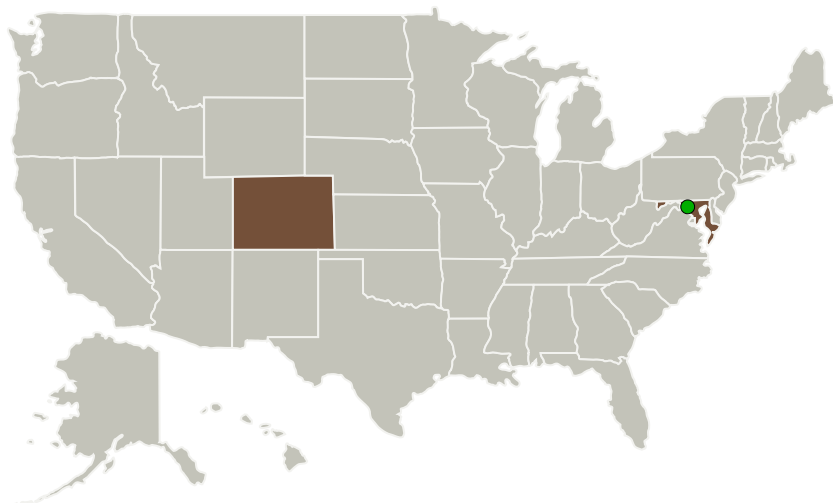
Project Introduction	1
Primary U.S. Work Locations and Key Partners	2
Project Transitions	2
Organizational Responsibility	2
Project Management	2
Technology Maturity (TRL)	2
Technology Areas	3
Target Destinations	3

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Primary U.S. Work Locations and Key Partners



Organizations Performing Work	Role	Type	Location
Microelectronics Research Development Corporation	Lead Organization	Industry	Colorado Springs, Colorado
● Goddard Space Flight Center(GSFC)	Supporting Organization	NASA Center	Greenbelt, Maryland

Primary U.S. Work Locations

Colorado

Maryland

Project Transitions

**February 2011:** Project Start**September 2011:** Closed out

Closeout Documentation:

- Final Summary Chart(<https://techport.nasa.gov/file/137916>)

Organizational Responsibility

Responsible Mission Directorate:

Space Technology Mission Directorate (STMD)

Lead Organization:

Microelectronics Research Development Corporation

Responsible Program:

Small Business Innovation Research/Small Business Tech Transfer

Project Management

Program Director:

Jason L Kessler

Program Manager:

Carlos Torrez

Principal Investigator:

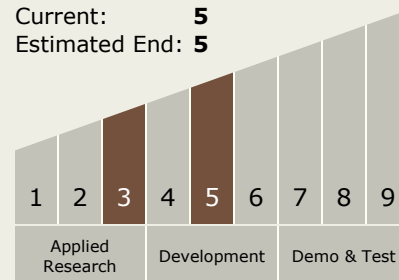
Xiaoyin (mark) Yao

Technology Maturity (TRL)

Start: 3

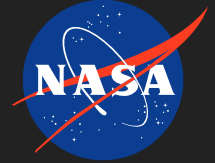
Current: 5

Estimated End: 5



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Technology Areas

Primary:

- TX02 Flight Computing and Avionics
 - └ TX02.1 Avionics Component Technologies
 - └ TX02.1.6 Radiation Hardened ASIC Technologies

Target Destinations

The Sun, Earth, The Moon, Mars, Others Inside the Solar System, Outside the Solar System